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5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RYAN LANE, EDWARD REYES,
MARK VEATCH and TOM GREGORICH

Appeal 2009-013954
Application 10/830,188
Technology Center 2800

Before SALLY C. MEDLEY, KRISTEN L. DROESCH and
KALYAN K. DESHPANDE, Administrative Patent Judges.

DROESCH, Administrative Patent Judge.

DECISION ON APPEAL

STATEMENT OF THE CASE

Qualcomm Incorporated ("Qualcomm"), the real party in interest, seeks review under 35 U.S.C. § 134(a) of a Final Rejection of claims 1-12 and 14. We AFFIRM.

BACKGROUND

Qualcomm's invention is related to microchip packaging. Spec. p. 1, ¶ 2; p. 2, ¶¶ 7-8.

Claim 1 is representative:

> A method for making a high pin-count die, comprising the steps of:
> providing a substrate;
> forming a die attach area onto the substrate for mounting a die, the die having at least one bond pad;
> locating at least one bond island onto the substrate;
> connecting the bond pad to the bond island with a wire bond; and
> connecting a plurality of solder balls to the at least one bond island, the plurality of solder balls being located inwardly from an edge of the substrate,
> wherein at least one redundant solder ball is used to form a path for the inner solder balls connected to bond islands to be electrically plated.

The Examiner relies on the following prior art:

Lin	5,468,999	Nov. 21, 1995
Chou	5,691,568	Nov. 25, 1997
Torres	5,898,213	Apr. 27, 1999

Claims 1-5, 11 and 12 are rejected under 35 U.S.C. § 103(a) as unpatentable over Torres and Lin.

Claims 6-10 and 14 are rejected under 35 U.S.C. § 103(a) as unpatentable over Torres, Lin, and Chou.

ISSUE

Did the Examiner incorrectly find that Torres and Lin describe connecting a plurality of solder balls to the bond island and a redundant solder ball used to form a path for the inner solder balls connected to the bond island to be electrically plated?

FINDINGS OF FACT ("FF")

1. Lin describes, referring to Figures 1 and 2 below, [numbers from Figures 1 and 2 inserted], a semiconductor die [12] mounted onto alternative package substrates [14], [16] that include a plurality of conductive traces [18] and a bond post [20] on one end and a conductive via or through hole [22] at the other end. Col. 3, ll. 33-37.

Lin's Figures 1 and 2 are below:

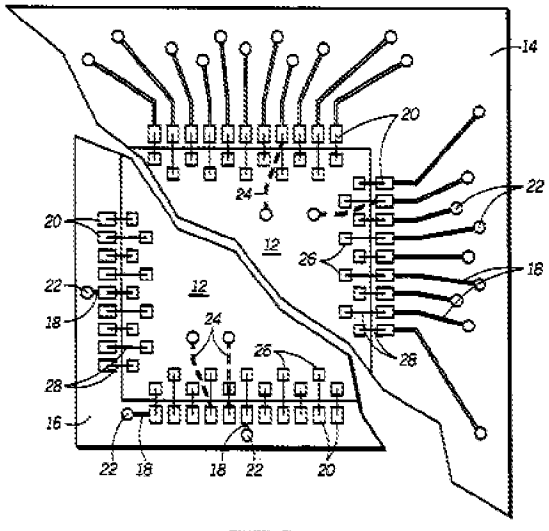

FIG.1

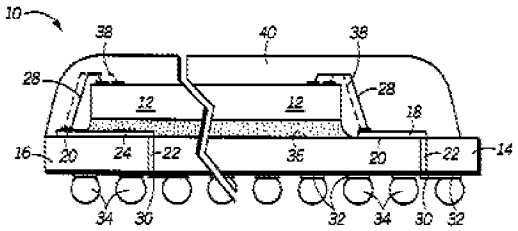

FIG.2

Figures 1 and 2 depict a die mounted on two different substrates.

2. The conductive traces [18] extend from the bond pads [20] outward, but can extend inward beneath the semiconductor die [12] as illustrated by phantom conductive traces [24] which terminate at conductive vias [22] located beneath the semiconductor die [12]. Col. 3, ll. 37-43.

3. Lin describes that substrate [14] has an outwardly extending conductive trace [18] and corresponding conductive via [22] and an inwardly extending conductive trace [24] and corresponding conductive via [22] connected to the same bond pad [20]. Fig. 1.

4. The conductive traces [18], [24] on the top of the substrate are routed through the substrate by way of conductive vias [22] and are further routed on the bottom of the substrate by a plurality of conductive traces [30] which terminate into conductive terminal pads [32]. Col. 4, ll. 53-55, 57-61.

5. Attached to each conductive terminal pad [32] is a conductive solder ball [34]. Col. 4, ll. 61-63.

6. Conductive traces [18] and bond posts [20] are formed on the substrate using conventional lithographic methods such as laminating or depositing a copper layer on the substrate, which is subsequently patterned by lithographic masking and etching and then plating the copper pattern with gold or a combination of nickel and gold. Col. 3, ll. 53-59.

7. Conductive vias [22] are formed using conventional processes such as drilling holes through the substrate followed by deposition of copper and nickel and gold plating on the sidewalls of the holes. Col. 3, ll. 59-62.

ANALYSIS

Independent claims 1 and 12 each recite: "connecting a plurality of solder balls to the at least one bond island . . . wherein at least one redundant solder ball is used to form a path for the inner solder balls connected to bond islands to be electrically plated." Qualcomm disputes the Examiner's finding that Torres and Lin describe the claim limitations arguing that neither Torres nor Lin alone or as combined describe or suggest connecting the solder balls and using at least one redundant solder ball to form a path for the inner solder balls connected to bond islands to be electrically plated. Br. 6-8. The Examiner does not interpret the wherein clause as including a positive recitation of a path for the inner solder balls to be electrically plated. Ans. 7. Rather, the Examiner interprets the wherein clause to only require that the redundant solder ball be capable of providing a path for the inner solder balls. Ans. 7. The Examiner finds that due to the placement of Lin's additional or redundant solder balls they are capable of providing a path for inner solder balls to be electrically plated. Ans. 7-8.

Even assuming that Qualcomm is correct that the wherein clause is a positive recitation of a path for the inner solder balls to be electrically plated, we find that Lin describes the disputed limitations. Contrary to Qualcomm's argument that Lin only describes a ball grid array having a solder ball [34] for each of the conductive terminal pads [32] (Br. 8), Lin also describes that one of the bond islands [20] (i.e., bond pad) on substrate [14] is connected to two solder balls [34]. In other words, Lin describes a path between a first solder ball [34] and a second solder ball [34] through the single bond island (i.e., bond pad [20]). The single bond island [20] is connected to an outwardly extending conductive trace [18] which is routed through and

along the bottom of substrate [14] by via [22] and conductive trace [30] and terminates at a terminal pad [32] attached to a solder ball [34]. Col. 3, ll. 37-43; col. 4, ll. 53-63; Figs. 1-2; FFs 2-5. The single bond island [20] is also connected to an inwardly extending conductive trace [24] (Fig. 1) routed through and along the bottom of the substrate [14] by via [22] and conductive trace [30] and terminates at terminal pad [32] attached to a solder ball [34]. Col. 3, ll. 37-43; col. 4, ll. 53-63; Figs. 1-2; FFs 2-5. Lin further describes that the redundant or outer solder ball [34] (connected by conductive trace [18] and via [22]) is used to form a path for an inner solder ball [34] (connected by conductive trace [24] and via [22]) to be electrically plated because Lin describes that the conductive traces, bond posts [20] and vias [22] that comprise the path are formed using plating. Col. 3, ll. 53-62; FFs 6-7.

Qualcomm additionally argues that there is no motivation to substitute Torres's solder balls with Lin's solder balls [34] and terminal pads [32] because Torres already describes solder balls and conductive terminal pads. Br. 8, citing Torres col. 5, ll. 30-31. Qualcomm's arguments are misplaced because the Examiner does not propose substituting Torres's solder balls with Lin's solder balls [34] and terminal pads [32]. Rather, the Examiner proposes modifying the teachings of Torres by connecting a plurality of solder balls where one solder ball can be used to form a path for an inner connected solder ball to be electrically plated as taught by Lin to increase the number of input/output terminals without causing electrical shorts and without increasing the size of the package. Ans. 4-5. For the same reasons explained before with respect to Lin, we are also unpersuaded by Qualcomm's argument that the hypothetical system of Torres in view of Lin

would provide a ball grid array with Lin's solder balls and a corresponding terminal pad and would not provide a ball grid array with at least one redundant solder ball which is used to form a path for the inner solder balls connected to bond islands to be electrically plated. Br. 8-9.

For all these reasons, we sustain the rejection of claims 1-5, 11 and 12 as obvious over Torres and Lin. Since Qualcomm does not present separate arguments addressing dependent claims 2-11 and 14 (Br. 9), we sustain the rejection of claims 6-10 and 14 as obvious over Torres, Lin and Chou for the same reasons.

DECISION

We AFFIRM the rejection of claims 1-5, 11 and 12 under 35 U.S.C. § 103(a) as unpatentable over Torres and Lin.

We AFFIRM the rejection of claims 6-10 and 14 under 35 U.S.C. § 103(a) as unpatentable over Torres, Lin and Chou.

TIME PERIOD

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

ELD